COPPER ELECTROPLATING PROCESS FOR MSAP RESISTANT TO ETCH-INDUCED PITTING

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ABSTRACT

The rollout of 5G technology is leading electronics circuity and IC substrate manufacturers to require higher densities in their designs. Due to the nature of 5G applications, high reliability and exceptional electrical performance in these designs are also increasingly important. To meet these needs, fabricators have gradually established the manufacturing capabilities to build boards using modified Semi-Additive Processing (mSAP). The copper plating electrolyte for mSAP needs to fill blind micro-vias, plate fine lines, and plate through holes simultaneously. One of the challenges in mSAP, however, are V-pits generated in the electroplated copper surface during the final flash etching step. Since these pitting defects might severely reduce the reliability in the final product, an additional baking step is currently used in the process flow to anneal the plated copper. This baking step takes several hours, increasing costs and decreasing throughput significantly. Therefore, innovative copper electroplating solutions that can provide via filling and fine line plating resolution capabilities and a copper deposit that can be etched uniformly across the surface during the flash etching step are desirable. The purpose of this study was to investigate the underlying pitting mechanism and to develop such a plating process to reduce pit formation. The factors that have effects on pitting formation, such as the type of plating electrolyte including additive package selection and optimization, etching rate and baking condition are discussed. The developed plating process, MacuSpec VF-TH 300, showed excellent via fill capability, great fine line resolution, and high throwing power for through hole plating in a single bath. The tensile strength and elongation of the deposit exceed the IPC class III requirements.

INTRODUCTION

The rollout of 5G technology is leading electronics circuity and IC substrate manufacturers to require higher densities in their designs. Due to the nature of 5G applications, high reliability and exceptional electrical performance in these designs are also increasingly important. To meet the needs of 5G applications and other next generation device platforms, fabricators have gradually established the manufacturing capabilities to build boards using modified Semi-Additive Processing (mSAP). Besides mSAP, Semi-Additive Processing (SAP) and Embedded Trace Substrate (ETS) processing, are also used to meet the requirements on the fabrication of fine features [1]. Since mSAP starts with a board that has thin copper foil laminated onto organic prepreg, the interconnects can provide higher reliability because of good adhesion of fine lines to the substrate. The main concept behind mSAP is to minimize the amount of copper buildup at each stage of the process, ultimately minimizing the total final amount of copper required to be etched away for circuit formation. This is referred to as the "copper budget" of the mSAP process. The typical mSAP process flow begins with an organic substrate clad with a very thin copper foil of approximately 3µm in thickness as shown in Figure 1. Microvias are then laser-drilled and the panels desmeared to clean any resin residues from the target pad and impart some topography to the via walls for adhesion of subsequent deposits. The panels are then processed through a primary metallization process such as electroless copper, a carbon-based direct metallization, or a conductive polymer to make via walls initially conductive. This is then followed by an imaging process and pattern plating with an acid copper electrolyte. The pattern plating is done both to fill the microvias completely with copper and build the copper traces to the required height. After plating, the resist is stripped off and a differential or flash etch is processed to form the final circuitry. Since it is the goal of each step to control the amount of copper deposited throughout the process, a typical total of only 2 to 3µm of copper is removed in the flash etch. This minimal copper etching preserves the profile of the circuit traces, permitting the production of finer lines. Multiple layers are then built up using prepregs tailored to mSAP processing. This series of processes offers fine lines with much greater precision, yielding fine lines with rectangular cross-sections that maximize circuit density and enable accurate impedance control with lower signal loss.

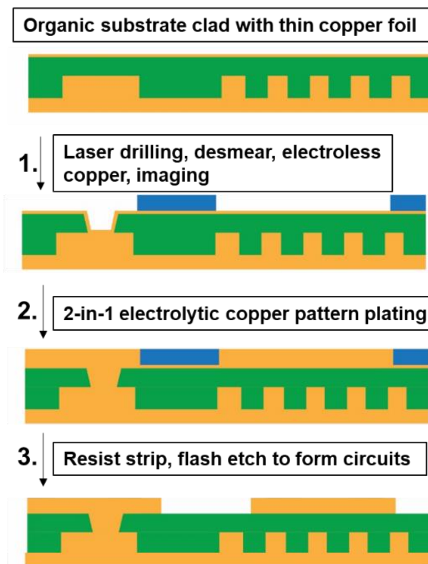


Figure 1. Typical mSAP process flow

One of the challenges in mSAP, however, is in the flash etching step, during which uneven etching, pinhole formation, pitting, and V-pitting, become significant issues. These defects can cause severe reliability issues in the final product, such as poor stacking over pits or pinholes, reduction in fine line cross-sectional area resulting in poor signal propagation, and creation of stress points that lead to potential cracking. Figure 2 shows the pits that are typically observed after etching on conventional electrolytically deposited copper. This phenomenon is called "V-pitting" due to the characteristic V shape of the pit. When observed from above, typical

pits on the surface appear circular. When they are cross-sectioned, the characteristic "V" shape can be seen. In this study, we focused on the formation and prevention of V-pits, although other pit geometries were also observed.

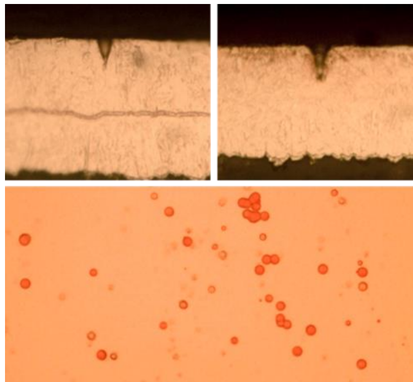


Figure 2. Surface with typical pitting image from above and a cross-section of pits showing the characteristic "V" shape

Many manufacturers observe these pits and have tried to mitigate them by annealing boards between plating step and etching step. However, this is time and energy intensive, reducing production throughput and increasing costs. Hence, creating an electrolytic plating system that reduces pits is highly desirable.

V-Pit Formation Mechanism

The mechanism by which voids form was investigated by Ho et al [2, 3]. They showed that the formation of these pits is correlated to contaminants in the Cu deposit. The contaminants cause channels or voids, which allow pits to form during etching, as in Figure 3.

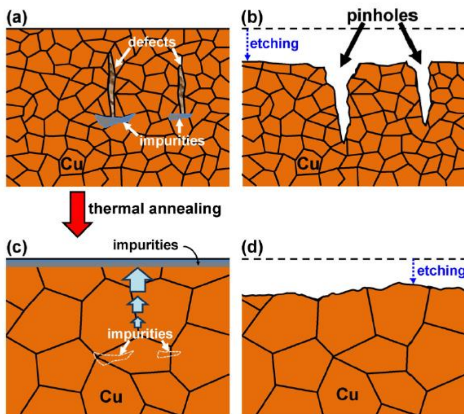


Figure 3. Pit formation mechanism

RESULTS & DISCUSSION

The results that were observed in the study agree with this mechanism. When intentionally applying contaminants to areas on the Cu clad surface prior to electrolytic plating, high volumes of V-pits were observed in these areas after plating and etching. Functional ingredients in the electroplating bath not only control the morphology, but also affect the rate at which organic impurities are incorporated into the deposited Cu. These ingredients include $CuSO_4$, Cl^-, H_2SO_4, wetters, levelers, and brighteners [4]. The type and amount of organic additives, including the wetters, levelers and brighteners play key roles on plating performance such as via filling capability, fine line shape, and the amount of V-pits formed during flash etching process.

Test Vehicle Plating and Etching

Performance of additive systems was determined by plating test panels and following reproducible etching procedures. Plating runs were carried out in 8L plating cell for additive screening, utilizing insoluble anodes in the plating cell. Electrolytes were made up, dummy plated for 1 Ah/L, and adjusted to specifications before plating panels. Each panel went through the standard cleaning and plating procedure shown in Figure 4.

Cleaner	Rinse	Acid Dip	Plating
Acid cleaner	DI water	10% vol H_2SO_4	Electrolytic bath
2 min. , 45 °C	2 min. , RT	1 min. , RT	50 min.

Figure 4. Pre plating cleaning and plating procedure

MacuSpec VF-TH 300 Process Selection

After screening the plated copper deposits from different types of additive packages for resistance on V-pit formation during etch step as well as the high performance required for via fill and fine line plating in mSAP, the MacuSpec VF-TH 300 electrolyte system was chosen for further optimization. The optimum operating conditions for balanced V-pit resistance, via fill, and through hole/fine line plating performance were determined by performing a DOE. Table 1 shows the resulting operating ranges and optimum levels in a VCP type of pilot plating tank, 500 L.

Table 1: Bath components, addition levels, and plating conditions

Parameter	Range	Optimum
Anode Current Density	1.0 – 3.5 ASD (10-32 ASF)	2.2 ASD (20 ASF)
Duration	Variable to target surface Cu	50 minutes
Temperature	20 - 27°C (68 - 80°F)	23°C (73°F)
Wetter	9 - 25 mL/L	10 mL/L
Brightener	0.25 - 1.0 mL/L	0.5 mL/L
Leveler	15– 35 mL/L	25 mL/L
Copper Sulfate ($CuSO_4 \cdot 5H_2O$)	230 - 250 g/L	250 g/L
Free Sulfuric Acid Electronic Grade	45 - 65 g/L	50g/L
Chloride Ion (Cl^-)	40 – 60 ppm	50 ppm

Under the conditions shown above, vias with dimensions of 100µm x 75µm, 100µm x 100µm, and 125µm x 100µm, were all filled with a dimple less than 10µm and a plated copper thickness of around 18 µm and through holes of 200µm x 800µm were plated with microdistribution and knee % greater than 80%. An example of typical and reproducible performance is shown in Figure 5.

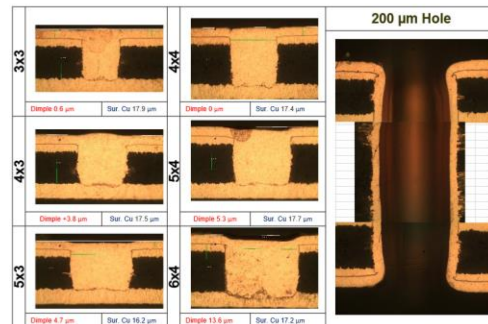


Figure 5. MacuSpec VF-TH 300 via fill and through hole plating

For a via size of 50 x 30 µm, it can be filled with slight bump of less than 5 µm, as shown in Figure 6.

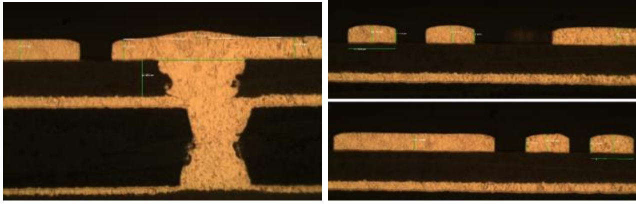


Figure 6. Via fill and the trace profile after mSAP processing

For the fine lines at 30 µm, the trace was plated well with trace profiles below 20%. Within each unit, the trace thickness variation is below 0.5 µm for the fine line widths of 30 µm compared to wider lines at 100 µm as shown above. The fine line thickness was about 15 µm after the flash etch step with an etching depth of 3 µm.

Flash Etching Procedure and V-pitting Evaluation

A proprietary peroxide-based etching solution was used to etch the Cu to the desired thickness for circuit formation. The etching solution was comprised of 10% peroxide (50% solution), 15% sulfuric acid, and 4% CircuEtch Additive. During etching, the solution was maintained at a temperature of 30(±2) °C. After plating was complete, panels were rinsed with DI water and dried with compressed air. Panels were allowed to sit for exactly 15 minutes at room temperature (21-24ºC). Flash etching was then carried out on the fresh deposit. The etching rate for this solution was ~ 3µm/30 sec. Separate samples from the panel were placed in the etching solution for 30 and 60 seconds, respectively, in order to etch 3 and 6 µm of the surface Cu. Finally, the pieces were dried with air and analyzed immediately under a microscope.

Conventionally deposited non-annealed Cu develops V-pits broadly across the surface after etching. The pits are both dispersed and concentrated in macroscale agglomerations. These V-pits occur on a such a large scale that it is not possible to quantify them. The etched surface of the non-annealed conventional Cu can be seen in Figure 7.

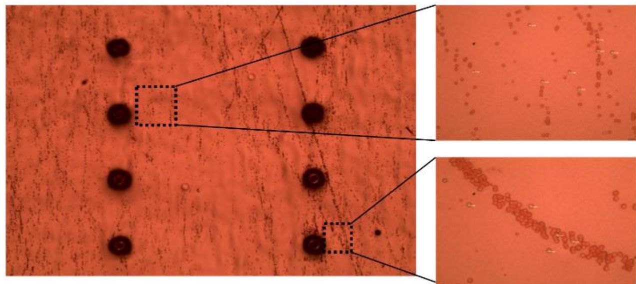


Figure 7. Non-annealed conventional Cu electroplated deposits after 3 µm flash etching. Isolated and bundled v-pits were observed.

The plating of MacuSpec VF-TH 300 electrolyte creates a surface that is very pit resistant. The number of pits on the surface is drastically reduced. Even without an exact quantitative method to evaluate the V-pit frequency, it is apparent from optical inspection that the number of pits on the surface is drastically reduced. Figure 8 shows the surface of the novel formulation after being etched.

During the plating experiments, it was observed that surface contamination on the board prior to cleaning can lead to surface defects in the electrolytically deposited Cu. These areas were more likely to have high concentrations of V-pits, especially if fingerprints were intentionally applied to the surface of boards to illustrate this. The novel electrolyte was less likely to have surface defects in these areas compared to the conventional acid copper products. Figure 9 shows panels that had fingerprints applied to the surface prior to cleaning, then were cleaned and plated. Surface defects can clearly be seen on the board plated using the conventional product, whereas MacuSpec VF-TH 300 creates a uniform deposit without defects.

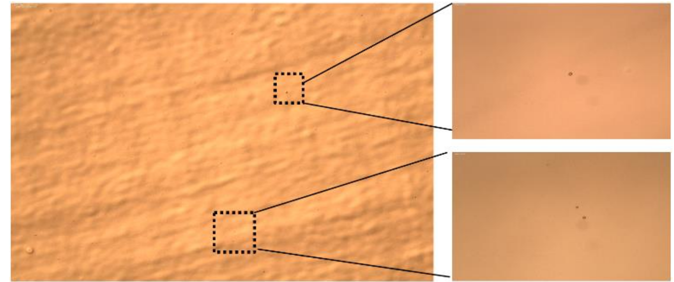


Figure 8. Non-annealed Cu deposit after 3 µm flash etching, plated with MacuSpec VF-TH 300. V-pits nearly eliminated.

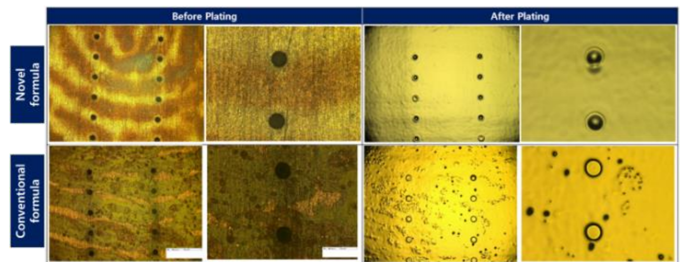


Figure 9. Panel surface where fingerprint was applied before and after plating.

The surface defects are also more prone to forming V-pits after etching. The areas that had fingerprints applied in Figure 9 were then etched down by 3, 6, 9, and 12 µm. The surfaces were then imaged as shown in Figure 10. The deposit plated from novel electrolyte etches very evenly, and no v-pits develop. The non-annealed conventional Cu deposit revealed V-pits after 3 µm of etching and these V-pits grow in size as etching continues.

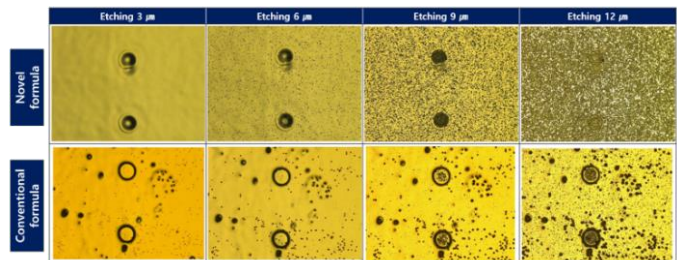


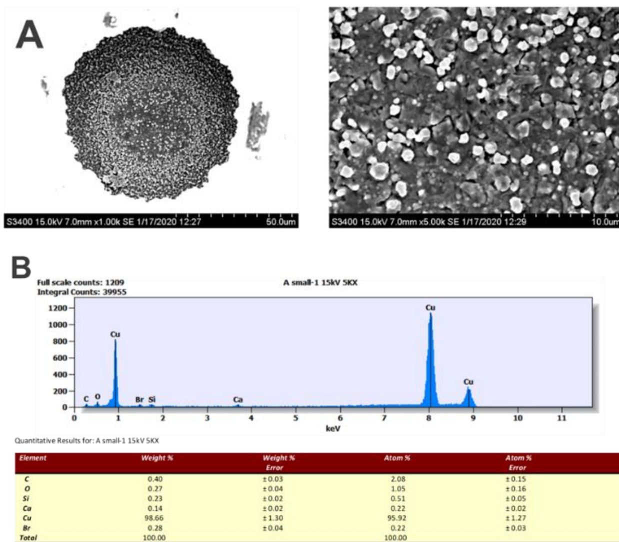
Figure 10 Fingerprint areas after surface etching.

Multiple types of test panels were utilized during the evaluations. Certain test panels had pits that formed specifically on filled microvias. We discovered that the identity of the boards and how they were processed influenced the preferential pitting of filled vias. Furthermore, the via diameter was correlated to the preferential pitting. Smaller vias were more likely to have pits than larger vias. Figure 11 shows examples of the preferential pitting of filled vias. The geometry of these preferential pits was not the typical "V" shape observed on the general surface and they were much deeper than typical.

Using SEM/EDS, the unplated boards were inspected for signs of contamination. Figure 12 shows the presence of contaminants including Br, Ca, C, O, and Si. The Si and O could be explained by glass bundles protruding from the side of the via, even though the

entire inside of the via should be covered with continuous Cu deposited by an electroless process. The presence of Br, Ca, and C are likely due to incomplete cleaning during board processing. We evaluated boards before and after our standard pre-plating cleaning procedure, and the contaminants were still present after cleaning, which indicates the resin smear could be at the bottom of the vias.

Figure 11. Preferential pitting on filled vias.



Element	Weight %	Weight % Error	Atom %	Atom % Error
C	0.40	±0.03	2.08	±0.15
O	0.27	±0.04	1.05	±0.16
Si	0.23	±0.02	0.51	±0.05
Ca	0.14	±0.02	0.22	±0.02
Cu	98.66	±1.30	95.92	±1.27
Br	0.28	±0.04	0.22	±0.03
Total	100.00		100.00	

Figure 12. A) SEM micrograph of a via from above showing the non-uniform bottom. B) EDS spectrum of the bottom of a via showing the presence of multiple contaminants.

Physical & Thermal Properties

It is critical that the deposited Cu is physically robust enough to withstand the physical demands of PCB applications. To evaluate this, the two primary physical attributes evaluated are tensile strength and elongation %. These properties correlate to the deposit's thermal stress tolerance. The organic additives (suppressor, grain refiner, and leveler) will affect these characteristic physical properties.

Tensile strength and elongation were measured according to the IPC TM-650, 2.4.18.1 standard. A stainless-steel panel was plated with MacuSpec VF-TH 300 electrolyte. Sample strips were then removed from the plated panel and baked in an oven at 125 °C for six hours. An Instron pull tester instrument was used to test the strips. The measurements were used to calculate tensile strength and elongation.
Tensile strength and elongation % of two separate samples were measured according to the IPC TM-650, 2.4.18.1 standard. One sample was plated when the bath was fresh, at 0 amp*hour/L and the other was plated after the bath was aged to 150 amp*hour/L. The results, shown in Figure 13, far surpass the IPC class III requirements (tensile strength > 36,000 psi, elongation > 18%). The novel formulation is very stable, with negligible change in performance between the initial and aged baths.

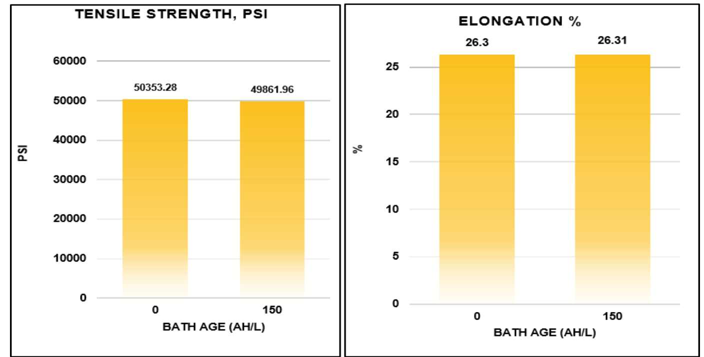


Figure 13. Physical properties of deposited copper when bath was initially made vs. when the bath was aged to150 amp*hour/L.

Solder shock resistance tests as per IPC TM-650 2.6.8 were conducted to study the thermal characteristics of plated boards. 3x and 6x solder shock tests were run using a 10 second float at 288ºC. The plated copper deposits met industry standards for solder shock resistance. Neither corner cracks nor barrel cracks were observed. The thermal integrity was excellent for all sizes of plated through holes and filled vias.

CONCLUSION

The plating process with chosen and optimized additives, MacuSpec VF-TH 300, showed excellent via fill capability, great resolution and uniformity on fine line formation in mSAP processing, and high throwing power for through hole plating in the same plating bath. The copper deposit from this process forms significantly fewer pits after a flash etching step, which can help solve the issue of pitting in circuit manufacturing without using time and energy intensive annealing processes. In addition to selection of appropriate additives that offer plated copper with pit resistance during the flash etch step, the study also indicated that surface contaminations play a role on pit formation. It was identified that that a properly cleaned surface prior to the plating process is also important to reduce the chance of pit formation during the etching step. Certain vias contained contamination, detected by SEM/EDS. When these boards were plated and etched, there was preferential pitting on the filled vias, even when utilizing the optimized electroplating formulation. However, the pitting was far less severe than that seen with non-annealed conventional formulations. The correlation between contaminants being incorporated into the deposited copper and the prevalence of pits in subsequent etching steps is in agreement with published literature.

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