FILLING CHRACTERISTICS OF PROCESS FOR ELECTROPLATING COPPER INTO MCROSCOPIC RECESSED FEATURES

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ABSTRACT
Copper is the most preferable metal used in electronic industry for filling small features. With the recent advances in copper electroplating it is possible to fill up blind micro vias (BMV) with electroplated copper. The effect of the electrolyte chemistry and the process parameters on the filling characteristics of copper electroplating has been studied. A preliminary treatment step is described that activate the interior surfaces of the small features leading to facilitating bottom-up filling. This activation step for bottom-up filling of vias reduces sidewalls growing that create seams/voids.

This paper also shows the results from a study of a novel process for filling through vias. Using electrodeposited copper to fill through vias in build-up core layers in HDI and IC with solid copper has an advantage in that its thermal and electrical characteristics are significantly better than any type of resin material available. The CTE of the copper-filled core is dependant only on the copper metal and the glass-reinforced resin of the drilled dielectric. The package substrate manufacturing process typically begins with a core layer that has through-hole connections. These through vias could be completely filled by using a modified process for acid copper electroplating. The operating parameters and the bath chemistry that includes high copper concentration and low acidity solution used for copper deposition are described in the paper. This technology is at an early stage being currently optimized to enable a variety of HDI and IC substrate package designs.

Key words: copper plating, blind micro-via, through hole filling

INTRODUCTION
Miniaturization and increased functionality demands have substantially decreased the sizes of electronic features that need to be plated. Copper is the most preferable metal used in electronic industry for filling small features due to its electrical and thermal conductivity properties and the possibility of electroplating. Vias that are not filled can lead to solder voids and reduced reliability. The conventional copper filling technologies are not capable of plating through holes at the same time as filling blind micro-vias due to the reliability problems.

Via filling by copper electroplating is an important technology in the fabrication of high density interconnections (HDI) of printed circuit board (PCBs) and IC package substrates [1-3]. New technologies started to develop in order to completely fill through vias in build-up core layers in HDI and IC with solid copper. Conventionally the through via holes in build-up core layers are plugged by using a thermally cured material after conformal copper plating. Next step is planarization by grinding and re-metallization by electroplating prior to dielectric build up. This is a labor-intensive multistep process. The mechanical abrading process after the resign cure can cause problems with the dimensional stability, particularly for substrate cores less than 100 microns thick. The new process for filling up through holes by copper electroplating has the benefits of improved thermal and mechanical properties as well as improved reliability. The productivity is increased by eliminating the separated steps of filing, planarization, and capping.

In this paper the effect of the chemical composition and the processing parameters on blind micro via filling characteristics of copper electroplating has been studied. The optimum conditions for filling up a wide range of micro via sizes are determined. The results obtained allow for enhancing via plating capabilities and increasing the reliability.

A process for filling pillars or bumps on substrates is also included in this paper. Further, a novel process for filling through via holes in core layers is described. Data enclosed demonstrate through vias in build-up cores filled without any voids and defects.

ACID COPPER PLATING PROCESS
A typical copper plating solution contains copper sulfate, sulfuric acid, chloride ions, and organic additives that control the deposition process and the quality of the plated coatings [4-6]. Various organic compounds are used in plating baths during the production of PCBs, chip carriers, and semiconductors [7, 8]. They act as levelers and brighteners enabling as uniform a deposition of copper as possible on different regions of the PCB including through holes and BMVs. The purpose of this work was to determine the effect of the organic additive species, their concentration as well as the processing parameters on via filling. In general there are three basic additives that are used in acid copper electroplating baths: Wetter, Brightener, and Leveler. The Wetter (suppressors, high molecular weight polyether compounds and polyoxyalkylene glycols)

in the presence of chloride ion has a strong polarizing influence producing a large decrease in the exchange current density. Addition of Brightener such as sulfopropyl sulfides to an acid copper electrolyte acts as a depolarizer producing an increase in exchange current density. As an example, the maximum depolarization effect for SPS (disodium bis (sulfopropyl) disulfide) was observed at a concentration up to 5 ppm. Above this concentration of the brightener, the surface blocking effect of the adsorbed brightener mitigates the depolarizing effect to some degree. The brightener spices are much smaller molecules than the wetter molecules and so the adsorption of the wetter does not appear to significantly interfere with the adsorption of the brightener. Leveler adsorbs preferentially near the most negatively charged sites of the cathode (PCB), thus slowing down the plating rate at high current density areas. The organic additives affect the secondary and tertiary current distribution and control the physical mechanical properties of the metal deposits.

PART 1
BLIND MICRO VIA FILLING

Test Vehicles

The tests vehicles included various via diameters in 4" x 4" grid, Figure 1. Side 1: vias 75 microns deep; via diameter 75, 100, 125, and 150 microns. Side 2: vias 100 microns deep, via diameter 100, 125, 150, and 175 microns; glass re-enforced dielectric. Through holes were interspersed with the grid. All via geometries were plated simultaneously.

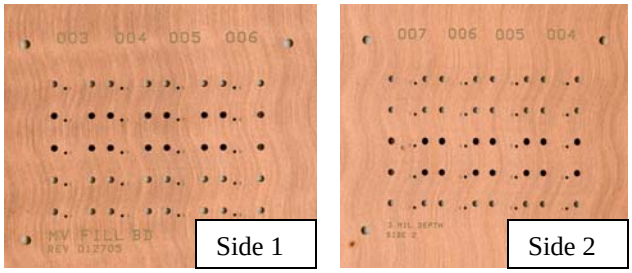


Figure 1. Test Vehicles

Via Fill Criteria

The Fill Ratio is defined as the ratio B/A in percents as shown in Figure 2.
Fill Ratio = B/A x100.
The acceptable value of the Fill Ratio is 80% or higher.

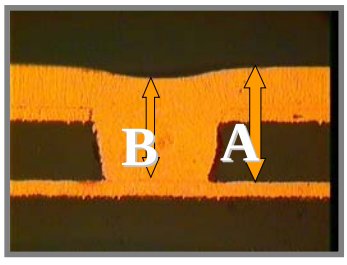


Figure 2. Fill Ratio

DOE

Experiment was designed (DOE) that included runs with various concentration levels of electroplating solution constituents and various plating conditions. Vis Fill organic additives were used, that included wetter - polyoxyalkylene glycol, leveler - a suppression agent, and brightener - a sulfur containing organic compound. A DC (Direct Current) plating regime was explored. Four factors were studied: copper ions concentration, brightener and leveler amounts in the bath, and preliminary treatment of the test vehicles in a pre-dip bath. Four concentration levels of the bath constituents were included. The pre-dip was a categorical factor – two levels – "yes" – included in the process sequence flow or "no" – not included. The responses measured were the Fill Ratio, dimple depth, inclusions (voids) for various sizes diameter vias and the surface copper thickness. Each DOE sample was cross sectioned and measurements were taken.

The goal was to minimize the thickness of copper deposited on the surface, to minimize the dimple depth, to eliminate voids (void free filling) and to obtained an optimum Fill Ratio of 80% or higher. Thus enhancing via filling capabilities of the process could be achieved.

Results from DOE

The plots obtained after analyzing the data are shown in the Figure 3 to Figure 7.

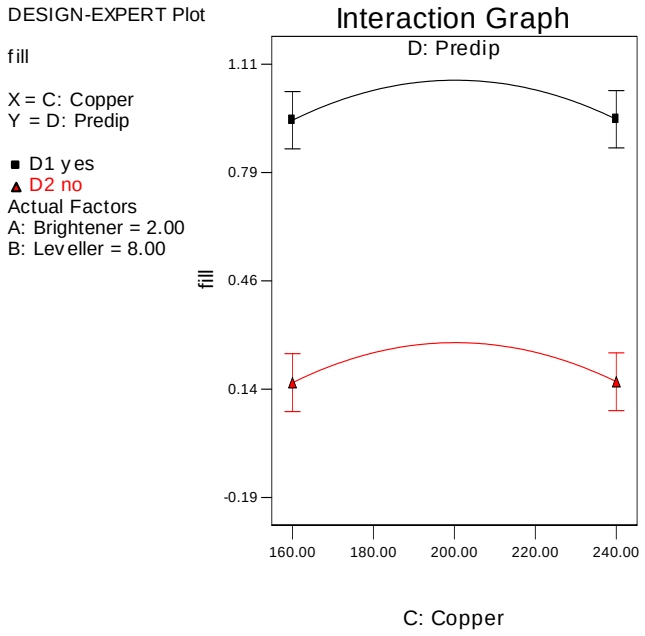


Figure 3. Fill Ratio as a Function of Copper Sulfate Concentration, g/l and Pre-dip for 75µm x 75µm vias. Brightener 2 ml/l, Leveler 8ml/l

Particularly important was found to be the interaction between the bath constituents and the process sequence. This can be seen form the Interaction graphs.

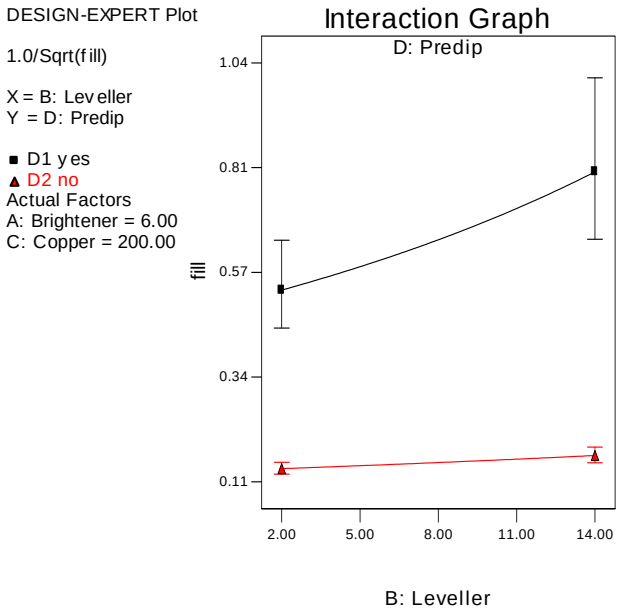


Figure 4. Fill Ratio as a Function of Leveler Concentration, ml/l and Pre-dip for 100µm x 100µm vias. Brightener 6 ml/l, Copper Sulfate 200 g/l

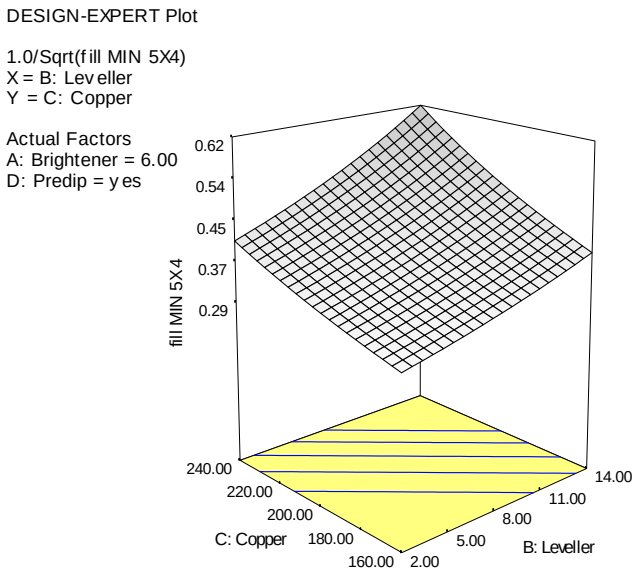


Figure 5. Fill Ratio as a Function of Copper Sulfate Concentration, g/l and Leveler Concentration, ml/l for 125µm x 100µm vias. Brightener 6 ml/l

The statistical results indicated the factors that were significant for filling up blind micro vias. The most significant factor was the use of Pre-dip. It reduced the dimple depth and increased the Fill Ratio considerably. Leveler concentration was found to be sometimes significant for filling vias. The optimization gave a recommended concentration of 14 ml/l for achieving high Fill Ratio and void free filling. Copper sulfate concentration was also found to be significant, the higher being the better.

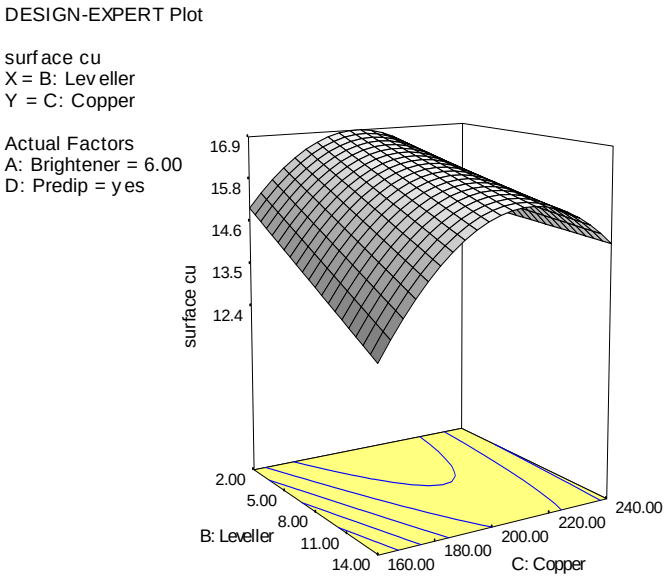
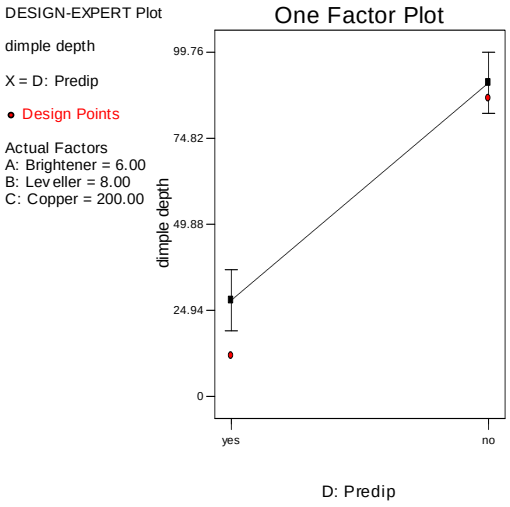


Figure 6. Surface Copper Thickness in microns as a Function of Leveler concentration, ml/l and Copper Sulfate concentration, g/l with Pre-dip. Brightener 6 ml/l

Surface copper thickness decreased as the leveler concentration increased form 2 to 14 ml/l with the pre-dip used, Figure 6.



Figure

Figure 7. Dimple Depth for 100µm x 100µm vias as a Function of the Pre-dip. Brightener 6 ml/l, Leveler 8 ml/l, and Copper Sulfate 200 g/l

The brightener concentration was found not to be significant for the responses tested.

The results from these experiments allowed optimizing the electroplating bath chemistry and the process sequence for filling up wide range of via sizes and minimizing the surface copper thickness.

The trough holes were plated as a part of this study to measure the physical mechanical properties and thermal characteristics of plated copper. The measured Tensile Strength of 41,000 – 42,000 psi and Elongation of 19 – 22% met the IPC specification. The reliability was evaluated by performing solder shock resistance measurements at 280 C for 10 seconds float, IPC 2.6.8. No corner neither barrel cracks were observed after 6x solder shock. Fine grained copper was deposited under the optimum plating conditions. The appearance of plated panels was bright and smooth.

Cross Sections

Cross section pictures shown in Figure 8 demonstrate various size vias filled up under the optimum plating conditions. They were pated simultaneously in a bath with high copper sulfate concentration of 240 g/L

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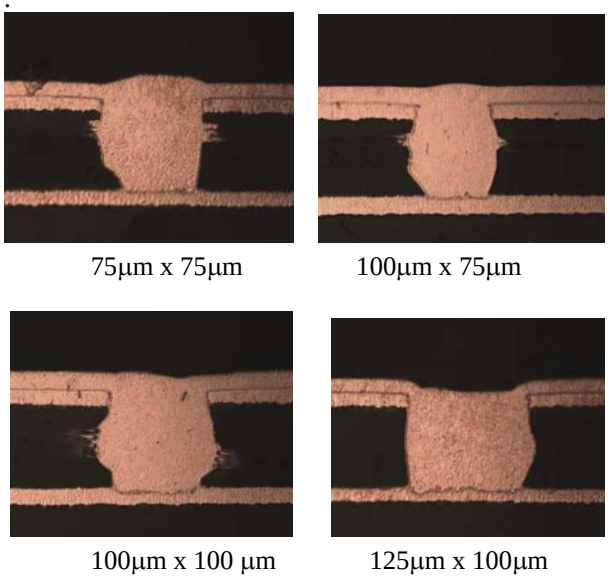


75µm x 75µm 100µm x 75µm

100µm x 100 µm 125µm x 100µm

Figure 8. Blind Micro Vias filled up in a Bath Containing Copper Sulfate 240 g/l, Leveler 8 ml/l, Brightener 2 ml/l

PART 2

FILLING PILLARS OR BUMPS ON SUBSTRATES

Electroplate Pillar Plating Process

The Electroplate BMP Pillar Plating Process has been studied. It is a DC acid copper plating system designed for filling photo defined pillars or bumps on substrates. The process combines the use of a copper activator with an electrolytic copper bath. The copper activation step is a combination of sulfuric acid and an additive used to ensure uniform pillar height.

Dry-Film Process

This is a crucial and important step in the process. The bumps are photo defined with a plating resist. This resist is typically thicker than standard plating resist used in the conventional PCB manufacturing and can be applied in a single or multiple pass through dry film lamination process. Dry film residues that are not removed from the base copper surface will result in low bump thickness or no bump plating at all.

Wetting of the Photo Defined Bump Areas

The aspect ratio of the intended plating areas may be up to and beyond a 1:1 aspect ratio. Plating resist by its very nature is hydrophobic (non-polar) and repels aqueous solutions, making "wetting" of the photo defined area more difficult. Proper cleaning chemistry, with low surface tension, is needed to ensure complete wetting of all holes.

Base Copper Activation

The base copper which will be plated must be dry film residue and oxide free. Uniformity of pillar height relies on quick and simultaneous copper plating initiation of all photo defined areas.

The optimized process ensures immediate plating initiation, yielding uniform bump/pillar height across the substrate.

Plating Results

Figures 9, 10 and 11 demonstrate plating of 4, 5 and 6 mils (100 microns, 125 microns, and 150 microns) diameter pillars.

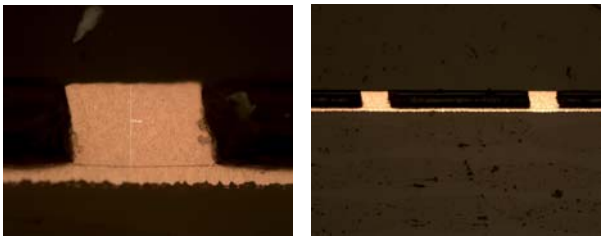


Figure 9. 100µm x 75µm Pillars

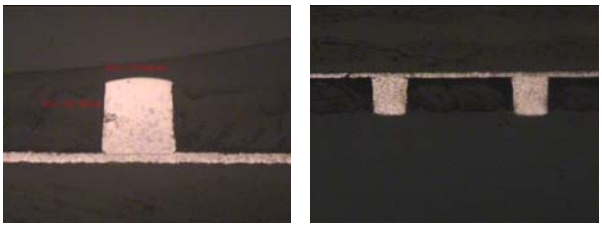


Figure 10. 125µm x 130µm Pillars

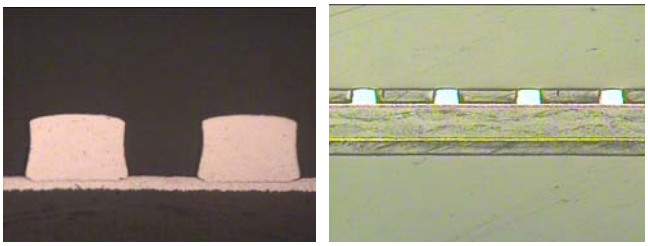


Figure 11. 150µm x 100µm Pillars

This process produces bright, fine grained, ductile deposits with excellent physical properties. It is applicable to Vertical Continuous Plater (VCP) or standard vertical plating equipment and could be used with soluble copper anodes or with inert anodes.

PART 3
THROUGH HOLE FILLING

The results from the study described above were used further in developing a novel process for filling through micro vias. Filling through via holes by copper electroplating started to develop recently to benefit the fabrication of printed circuit boards (PCBs) with high-density interconnections (HDI) [9] and three dimensional (3D) chip stacking [10]. Copper electro-deposition to fill through vias is particularly beneficial for the latest package substrates designs.

There are differences between the plating processes for filling blind micro-vias and through vias due to the differences in the geometric shapes. The differences include the hydrodynamic conditions, solution flow in and out of the through vias. Copper could be deposited in a center-up mechanism, as opposite to the bottom up mechanism in case of blind micro vias.

Test Vehicles for Through Hole Filing

The test vehicles used for through vias fill were 0.150 mm thick substrates. Hole diameters were 75, 100, 125, and 150 microns. Flexible 0.100 mm thick substrates with 100 microns hole diameter and flexible 0.050 mm thick substrates with 50 microns hole diameter were included in the tests. A case study plating of a 0.200 mm board with X shaped 60 micron diameters through via hole is shown as well.

Plating Conditions

Sulfuric acid copper bath was utilized. CuSO4x5H2O concentration was in the range 180 – 240 g/L, sulfuric acid concentration was 40 – 100 g/L, and Chloride ions were form 30 ppm up to 85 ppm. Tests were performed with soluble copper anodes and with inert anodes.

Various plating regimes were used, including DC plating with a CD (current density) from 8 ASF (0.86 ASD) up to 15 ASF (1.6 ASD), Pulse Reverse Plating, and combination between them. Hydrodynamic conditions: air sparger agitation and horizontal cathode rocking during the plating. The bath control and maintenance was performed by CVS analysis, volume analysis, and Hull cell tests.

Results and Discussions

The plated test vehicles were cross sectioned and evaluated. The responses were filling the holes with solid copper (accounting voids / inclusions if any), surface copper thickness, and dimple depth. The goal was to minimize the thickness of copper deposited on the board surface and to minimize the dimple.

Pictures of through hole sections were taken for each plating condition. Figure 12 and Figure 13 show cross sections of through via holes with various diameters in 150 microns thick test vehicles. The vias were filled up with copper without voids.

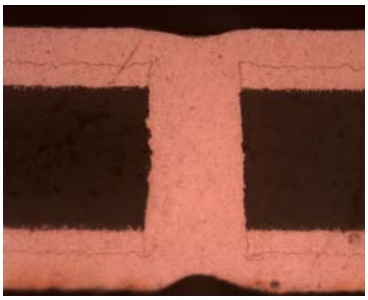
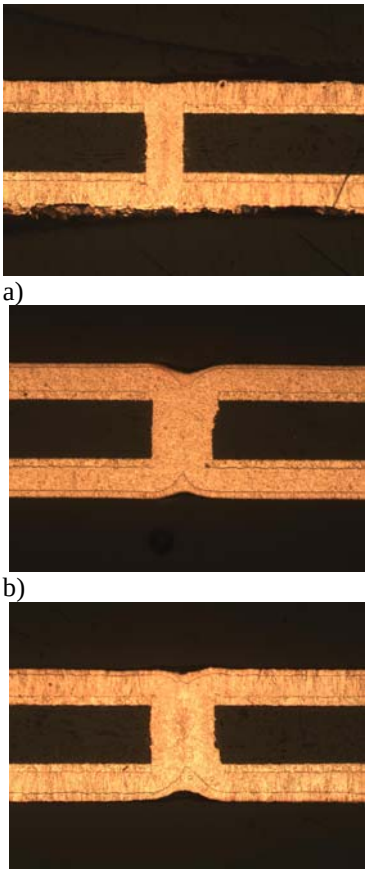


Figure 12. 75 μm diameter Through Via in 0.150 mm Thick Substrate, DC plating



a)
b)
c)

Figure 13. Through Hole Fill of 150 μm thick substrate; Hole diameter: **a)** 75; **b)** 100; **c)** 125 microns; PPR and DC

It was found that a higher copper concentration in the plating bath and a DC plating regime were beneficial for filling up the small diameter holes such as 75 micron diameter vias. For the larger diameter holes a lower copper concentration and a PPR regime or combination of a PPR and DC regimes were preferred.

The deposition rate on the hole walls, hole corners and on the surface depends on the plating conditions. As opposite to the BMV filling up, this rate was found to be higher in the center of the hole at the earlier stages of the plating. As the plating process continued further, the top and the bottom parts of the hole were filled up void free.

The hole filling process depends on many factors such as bath constituents, plating parameters: current regime, temperature, plating sequence; hole geometry, the pitch. In particular it was found that the smaller the pitch, more difficult was to fill up the through via holes. Thicker copper deposit on the surface was obtained in that case. This observation is shown on Figure 14.

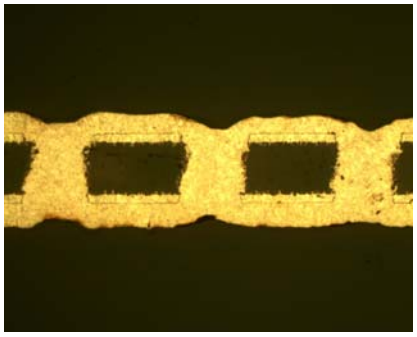


Figure 14. 100μm diameter Through Vias in 0.1mm Thick Flexible Substrate

In addition to that depending on the designs, different pitches on one board increase the difficulty to achieve an acceptable plating / filling.

Figure 15 demonstrates filing up of through via holes in 50 microns flexible substrate. The surface copper thickness is 17 microns.

Figure 15. Filling 50 μm diameter Through via holes in 50 μm thick flexible substrate

A thin surface copper plating was achieved in a case study with X shaped through holes. The center up filling mechanism was enhanced by the hole geometry resulting in a faster hole filling with less copper deposited on the board surface, as shown in Figure 16.

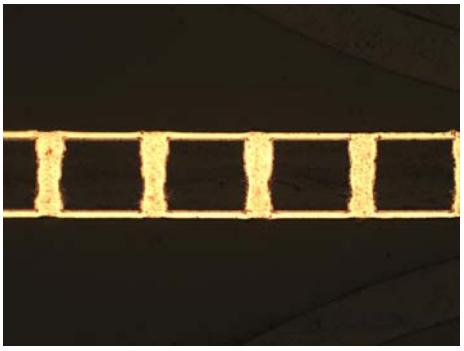


Figure 16. 60 μm diameter Filled up Through vias in 0.2 mm Thick Substrate, DC plating

The described innovative Through Hole Filling technology is at an early stage. It is at the process of further adjustments, chemistry and current regimes optimization to enable a variety of HDI and IC substrate package designs.

CONCLUSION

This process for filling microscopic recessed features with electrodeposited copper was optimized. The significant factors in blind micro via filling up were determined.

The results obtained from investigation of blind micro via filling process were used to develop electroplating processes for other applications. This includes a process for pillar / bump plating and filling through via holes process. The last one being further optimized in an effort to satisfy the latest requirements in the field.

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