# **RDL** and Pillar Fabrication from a Versatile Copper Plating Process

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# ABSTRACT

Advanced packaging suppliers are having two primary challenges during IC substrate fabrication. These challenges are not only in meeting the copper plating performance requirements but also in reducing manufacturing process costs. Copper plating processes must provide both high resolution and strict height uniformity within a unit/die (WIU) and within a wafer/panel. This is because the designs include features such as fine lines and pillars, whose top shape and coplanarity are critical to the product quality. To reduce manufacturing process costs, copper plating solution can be developed to plate multiple types of features in the same electrolyte, reducing the need for multiple plating tools. This flexibility allows fabricators to save on floor space, equipment and processing time.

In this paper, an electroplating package, Systek ETS, is introduced to plate both RDL and pillars under different current densities in vertical continuous platers (VCP). The plating uniformity and coplanarity of both RDL fine lines and pillars were evaluated on a panel level.

The Systek ETS package offered excellent coplanarity within a pattern unit for RDL plating. The variation in the plated height (or thickness) between fine lines of 5  $\mu$ m widths and pads 50  $\mu$ m widths respectively, was below 1.0  $\mu$ m when using a current density of 1.5 ASD. The tops of the fine lines have defined, rectangular shapes and their resultant profile offers excellent conductivity.

The same electrolyte package for pillar plating under higher current densities of around 5-10 ASD resulted in pillars with slightly domed profiles. These copper pillars had very good uniformity within unit and within panel.

Physical properties of the plated copper deposit are essential for the reliability of the finished product. A few key physical properties are tensile strength, elongation %, and internal stress. Copper deposited with the electrolyte package had tensile strength above 40,000 psi, elongation % above 18%, and internal stress below 1.0 Kg/mm2. The physical properties of the deposited copper did not change considerably during the bath aging, showing that the package had a stable performance over bath life.

The reliability of both pillars and RDL features were evaluated via solder dip at 288°C for 60 repetitions. The plated features did not show any crack or separation from the substrate.

# INTRODUCTION

Panel Level Packaging (PLP) is gradually being adopted to meet the packaging substrate supply chain requests of reducing manufacturing cost, but usage is still low due to application challenges for plating uniformity and limited packaging design adoption. Plating uniformity and specifically trace top planarity, which measures how flat the tops of the traces and other features such as pillars and vias are, represent important qualifying features of a copper plating process. A non-planar surface with fine traces could result in signal transmission loss, distortion of the connecting points, and possibly result in short circuiting of the device leading to catastrophic failures. Additionally, in pillar plating and RDL applications, any surface non-uniformity results in the requirement of a planarization step after plating that adds additional processing steps and costs. Therefore, copper plating solutions providing uniform, planar profile without any special post treatment are highly favorable options to fabricators for these two manufacturing processes. Due to the wide array of package designs being utilized today, which may include many kinds of features in advanced packaging, fabricators are interested in the ability to use one plating line to process multiple designs. In such a case, a single line / plating tool may be able to plate fine lines and to fill vias from in a single processing step under the same range of the current density or switch to plating fine lines and pillars with a change to a different current density range.

On the plating performance, a key problem to be solved is to obtain both high resolution and height uniformity within the RDL fine lines or pillars during copper plating process. In this paper, an acid copper plating process is introduced for the plating capability on RDL fine lines as well as pillars, under different current densities. The electrolyte was evaluated successfully on plating uniformity and coplanarity of both RDL fine lines and pillars on panel level scale plating with vertical continuous platers under conditions suitable for high volume production.

## **RDL Fine Line Plating**

For RDL fine line plating, an electrolyte branded as Systek ETS was used as shown below. The plating evaluation was completed in a vertical continuous plater (VCP). The test panels used were with a photo imaged dry film patterns on them, with a thickness of 25  $\mu$ m. Each test panel went through a pre-clean cycle of 1 min acid cleaner, 1 min rinse, and 1 min 10% sulfuric acid before plating in the acid copper containing the electrolyte as described below.

Systek ETS	Chemistry	Concentration	
	CuSO <sub>4</sub>	100 g/L	
VMS	H <sub>2</sub> SO <sub>4</sub>	200 g/L	
	Cl	60 ppm	
	Wetter	5 ml/L	
Additives	Brightener	2.5 ml/L	
	Leveler	10 ml/L	
Duranta	CD	1.0-7.0 ASD	
Parameter	Temperature	20-27 °С	

Table 1 Electrolyte and plating parameters

Typical acid copper electrolytes contain copper sulfate, sulfuric acid, chloride ions, and organic additives. These additives play a crucial role in controlling the deposit distribution as well as the physical properties of the copper deposit. To meet specific objectives of the plating process, these additives should be monitored and controlled properly. The additives work in combination when they are controlled within a given range to improve plating uniformity. Namely, these additives are the wetter (or suppressor), brightener and leveler. The wetter works in the presence of chloride ion to adsorb on to the cathode and increase the effective thickness of the diffusion layer. Therefore, the plating current increases and the deposit becomes more uniform, and a densely packed copper deposit can be obtained without burning. This modified diffusion layer improves the distribution of the deposit especially in fine line plating. The brightener is also called the anti-suppressor and as the name implies, it reduces the suppression. Most importantly it also acts as a grain refiner to deposit copper with a fine grain structure in random orientation. Therefore, the brightener has the most influence on final structure and physical properties of the deposit, such as tensile strength and elongation.

The leveler is a mild suppressor that adsorbs onto specific locations such as corners and peaks of base materials and aids in leveling the thickness of copper deposit. In the presence of a micro profile, the diffusion layer tends to be thin at the peaks and thick at the valleys. In this case the micro profile will be exaggerated if it is plated without a leveler. On the other hand, the plating on the peaks will be suppressed and the micro profile will be diminished if a leveler is present. Therefore, the additives play key roles to obtain plating uniformity and physical properties. In addition to the selection and optimization of the additives, the type of anodes in the VCP, the VMS make-up, and the current density also have significant effects on plating performances.

The following is an example of the influence of plating uniformity

Systek ETS Soluble anode	Line thickness(µm)				Pad thickness (µm)			Thickness variation R (μm)	
Fine line (µm)	1	2	3	avg.	1	2	3	avg.	(line-pad)
7/7	17.82	18.03	17.73	17.86	19.45	19.16	19.16	19.26	1.40
5/5	17.14	17.86	17.37	17.46	20.14	19.55	19.26	19.65	2.19
	Line thickness(µm)								
Systek ETS Insoluble anode		Line thic	kness(μm)			Pad thic	kness (μm)		Thickness variation R (µm)
Systek ETS Insoluble anode Fine line (µm)	1	Line thic	ekness(μm) 3	avg.	1	Pad thic 2	kness (μm) 3	avg.	Thickness variation R (μm) (line-pad)
Systek ETS Insoluble anode Fine line (µm) 7/7	1 19.02	Line thic 2 18.5	ekness(μm) 3 19.02	avg. 18.85	1 19.53	Pad thic 2 19.53	kness (μm) 3 19.53	avg. 19.53	Thickness variation R (µm) (line-pad) 0.68

 Table 2. Plated height variations between fine lines and pads

from the type of anodes utilized in the VCP. In this testing, the plating current density was 1.5 ASD, and the plating time was 60 minutes to obtain a copper thickness around 20  $\mu m$ . The plated height variation between fine lines of 5 and 7  $\mu m$ , and the pads was measured from cross sections as shown in Figure 1.

Figure 1. Cross sections of fine lines from the plating process with insoluble anodes

Fine lines at 7/7 μm	Fine lines at 5/5 μm			
Librib.617 um Librib.500 um Librib.500 um Librib.617 um Librib.531 um Librib.531 um Librib.531 um Librib.531 um	L38=17.989 um L37=19.017 um L36=17.989 um L38=19.017 um L36=19.017 um L39=19.531 um			
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When the VCP was operated using soluble anodes, the plated height variations between fine lines and pads were 1.4 µm for the unit with fine lines at 7  $\mu$ m and 2.19  $\mu$ m for the unit with fine lines at 5 µm. Switching to insoluble anodes, the plated height variations between fine lines and pads were all below 1.0 µm for both units with the same 7  $\mu$ m and 5  $\mu$ m line size as shown in Table 2. Besides higher plating uniformity, insoluble anodes are also easier to maintain and are capable of higher plating current densities as discussed in the pillar plating section of this paper. Thickness variation across the 410 mm x 510 mm panels, was measured at 3 points, from top, middle to bottom, as shown in Table 3. For the fine lines at 10 µm, the plated copper height variation was found to be below 0.5 µm when plating under a current density of 1.5 ASD. The thickness variation was approximately 1 µm under a higher plating current density of 4 ASD. It is common knowledge that plating uniformity can be improved when plating current density is reduced.

Table 3. Plated height variations between fine lines and pads within unit as well as within panel

	Pad			Pad Pattern				R value			
	1	2	3	4	Aver.	1	2	3	4	Aver.	μm
Тор	19.43	19.54	19.49	19.43	19.47	18.76	18.98	19.15	19.32	19.05	0.42
center	19.43	19.26	19.43	18.93	19.26	18.98	18.99	19.04	18.65	18.91	0.35
bottom	19.82	20.10	19.77	19.88	19.89	19.71	19.60	19.71	19.48	19.63	0.26

5G+

## **Pillar Plating**

Successful pillar plating is even more challenge on height uniformity than fine line RDL plating due to higher current density applied to reach the pillar height within an acceptable plating window. Additionally, the differences in electrochemical potential across each die further increases this difficulty. The plated pillar is higher at the edge and corners, resulting in taller bumps at the edge, especially on die with high bump densities. The variation increases when there are pillars with different diameters within a die as well. To overcome the uniformity issues within die, a polishing step is normally required after the mold compound is applied in fabricating processes. This results in additional steps and higher costs depending on the uniformity requirements. Furthermore, a flat or slightly domed pillar shape is preferred in subsequent final finish processing. The uniformity on pillars is calculated according to the formula:

# Uniformity (WID%) =[(Height<sub>max</sub>-Height<sub>min</sub>)/Height<sub>avg</sub>]/2\*100

The same Systek ETS system was tested for pillar plating to examine the feature uniformity under current densities of 5 and 7 ASD, with plating times of 66 minutes and 44 minutes, respectively, in the same electrolyte as discussed in fine line session. A WYKO profiling instrument was used to measure the feature shape and plated uniformity within a die.

The WIF uniformity was good, with all measurements below 3.5 um under the process conditions. For the current density of 7 ASD, WIF% was below 4.7%, and it dropped further to below 2.0% when current density was reduced to 5 ASD. This is shown in Table 4 and Table 5.

Table 4	Uniformity	measurement under 5 ASD
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To test the uniformity within a die, a panel with differing diameters of pillars and pads was used. This panel plated under a current density of 7 ASD for 170 minutes to obtain a pillar height of 200  $\mu$ m. Great uniformity of 1.3%, was achieved within unit as shown in the Table 6.

Table 7. Thickness measurements on the plated panel

Loc	ation	Wyko measurement		WIF (um)		Avg (um)
1	X axis	Mexco	0.74	2.18	3.42	2.50
	Y axis		1.95	4.5	2.77	2.09
2	X axis	Veros	4.41	3.6	2.37	2.5
2	Y axis		5.03	2.7	3.35	3.5
0	X axis	Veco III	3.35	3.38	2.11	0.40
3	Y axis		1.41	0.63	2.25	2.18

Table 6A. WIU uniformity measurement under 7 ASD



Table 6B. WIU data

Figure 2. Full panel measured at 5 ASD



The uniformity within unit can be improved further to around or below 1% under current densities of 5 ASD to obtain pillar heights of around 150  $\mu$ m as shown in Figure 2.

The data in the table 7 shows the uniformity on a  $410 \times 510$  mm panel under the same plating conditions. The uniformity within this panel was about 7.1%. After mold compound process, thermal

	Location-1	Location-2	Location-3	Location-4	Location-5	Location-6	Location-7		
	148.69	144.36	147.69	155.25	165.45	164.78	146.03		
	148.36	145.14	146.48	153.57	166.44	163.34	146.03		
Plated Thickness	148.03	144.81	145.70	153.13	167.67	162.12	146.48		
	148.25	146.25	145.03	153.13	167.67	163.12	143.15		
	147.47	146.80	145.03	153.35	167.67	164.00	144.03		
average	148.16	145.47	145.98	153.69	166.98	163.47	145.14	Full panel average	152.70
R	1.22	2.44	2.66	2.12	2.22	2.66	3.33	Full panel Rmax	21.84
%WIU	0.4%	0.8%	0.9%	0.7%	0.7%	0.8%	1.1%		

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# Figure 3. Panels before solder dip (left), Panels after solder dip (right), inspected by SAM

Figure 4. Copper deposit FIB/SEM pictures under different plating current densities.



stress, 288°C solder dip, 60 times, no separation was observed from scanning acoustic microscope (SAM) inspection as shown above in Figure 3.

### **Copper Deposit Physical Properties**

Physical properties of the plated copper deposit are essential for the reliability of the substrate. A few of the most important physical properties are tensile strength, elongation %, and internal stress. These properties show the tolerance of the deposit for thermal stress and warpage. The wetter, brightener, and leveler additives influence the physical properties of the deposit. Standard testing equipment was used to measure the tensile strength, elongation %, and internal stress. Tensile strength was above 40,000 psi and elongation% was above 18%. Internal stress is an important parameter when plating thin RDL. With high internal stress, the deposit may warp, and warpage may get worse with time or with temperature. The internal stress of the plated deposits using system at current densities of 1, 4, 10 and 15 ASD was measured, and all exhibited low stress below 1.0 Kg/mm2 after annealing at 180 °C for one hour.

#### Chart 1. Internal stress



#### **Copper Deposit Grain Structure**

An X-Ray Diffraction (XRD) study was performed for the plated deposits under current density of 1.5 ASD to identify the crystal phase and different planes. The diffraction pattern obtained was

the same as the standard reported in the literature. Besides the relative intensities of the crystal orientations, the crystallographic density and lattice constant, also of interest is whether there is a preferred orientation. The data indicates that the deposits from the bath have preferred [111] planes as shown in the Figure 5.

Figure 5. Copper deposit XRD data

Various data	Lit. Value Cu	Systek ETS 1200
111	100	100
200	46	11.4
220	20	10.7
311	17	5.5
Lattice constant a [Å]	3.615	3.609
Density [g/cm³]	8.92	8.98
Stress [MPa]		-6.7 ± 4.7

The FIB-SEM photos in Figure 4 above show that the plated copper deposit had equiaxial grain structure, and that it does not vary significantly whether plated under different current densities.

#### CONCLUSION

We presented copper plating processes for fine line plating and pillar plating for package substrates. The objective was to achieve coplanarity and uniformity within unit and within panel. The electrolyte utilized demonstrated the capability to plate fine lines with excellent coplanarity between the fine line feature height and pad feature height. The electrolyte also showed great uniformity on pillar plating when higher current density was employed, depositing plated pillars with slightly domed shapes. The physical properties, tensile strength and elongation passed IPC class III specification. Low internal stress was shown for both applications as plated and after annealing. All of the additive components were able to be analyzed with Cyclic Voltammetry Stripping analysis.

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